LOW DC POWER MONOLITHIC LOW NOISE AMPLIFIER FOR WIRELESS APPLICATIONS AT 5 GHz

Urs Lott

Swiss Federal Institute of Technology (ETH) Zürich,
Laboratory for EM Fields and Microwave Electronics,
Gloriastr. 35, CH-8092 Zürich, Switzerland,
Fax + 41 1 632 11 98, e-mail: lott@ifh.ee.ethz.ch

ABSTRACT

A two stage monolithic integrated low noise amplifier for applications in the wireless data frequency range of 5 to 6 GHz has been designed. A noise figure of 3.5 dB with a gain of 15 dB has been achieved using enhancement MESFETs only. The LNA draws 3 mA from a 3.3 V supply, achieving a gain/P_{DC} figure of merit of 1.5 dB/mW.

INTRODUCTION

For portable wireless data applications the power consumption of the receiver has to be minimized, because the receiver is usually running for much longer time than the transmitter. There are a number of proposals for wireless data systems in the 5 GHz range, e.g. in the 5.8 GHz ISM band in the US, and 5.2 GHz Hiperlan in Europe. These systems demand for low noise amplifiers (LNAs) with low DC power consumption.

There have been a number of recent papers on low power LNAs in the range of 900 MHz/L-band [1,2] and S-band [3,4,5]. Generally the lowest noise figures are obtained with heterojunction FETs (HEMTs) or bipolar transistors (HBTs). LNAs in the 2.4 GHz range achieve a noise figure of 1.5 to 3 dB with a gain/P_{DC} figure of merit of between 0.3 and 4 dB/mW [3].

At 5 GHz little reference data is available, yet one expects a slightly higher noise figure and a lower gain/P_{DC} figure of merit. Recently, an HBT amplifier with 2.9 dB noise figure and 16 dB gain at 5.7 GHz has been reported [6]. Its DC power consumption is 72 mW, which gives a gain/P_{DC} figure of 0.23 dB/mW.

Ultra low noise figure is generally not necessary in short range wireless applications. The emphasis of this work is to reduce power consumption of the LNA while still having acceptable noise performance (NF < 4 dB).

In commercial and consumer applications cost must be kept low. Thus chip size must be minimized and a foundry process with proven yield and reliability must be used.

The LNA presented in this paper achieves a noise figure of 3.5 dB at 5.2 GHz with a gain of 15 dB using the enhancement device of a standard E/D-MESFET foundry process. The measured variation of the noise figure over 10 devices from two different wafers is less than 0.25 dB.

For compatibility with low power CMOS circuits and PCMCIA cards, a single 3.3 V supply voltage is used. Power consumption is 10 mW (3 mA from a 3.3 V supply), yielding a gain/P_{DC} ratio of 1.5 dB/mW. This would even place the presented amplifier in the better half of the comparison chart shown in [3] for the lower operating frequency of 2.4 GHz.

CIRCUIT DESIGN

The enhancement MESFET of the process used has higher gain per mA of DC current than the depletion device. However, the gate bias voltage has to be controlled carefully to prevent excess gate current flow which degrades the noise figure.

DC feedback is used together with a resistive load impedance in the first stage to stabilize the bias point (see the schematic diagram, Fig. 1). The same bias voltage can be used for the second stage by bridging the interstage coupling capacitor (Ck2) with a 7kΩ

resistor. Simulations have shown that the noise contribution of these bias resistors is negligible.

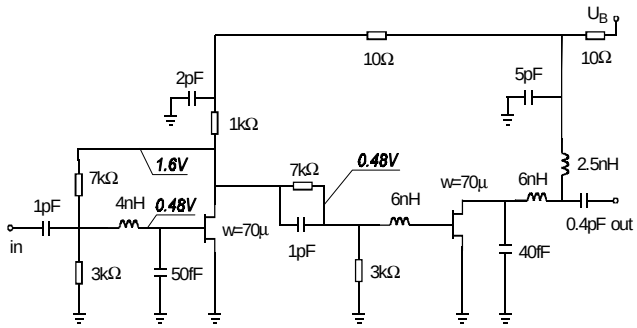

Fig. 1: Schematic diagram with nominal bias voltages at U_B = 3.3 V

All resistors used for DC bias point stabilization are made with the same implant to limit the influence of process variations.
Inductive matching is used at the ports and for interstage matching. The 5 GHz range is actually very well suited for chip inductors which have a quality factor Q of around 10 at 5 GHz in this process. To match the input and output impedances to 50 Ω, additional capacitors are used. Thus, a smaller active device with lower bias current can be used. The gate length of the FETs is 0.7 µm and the width 70 µm. The nominal bias current per stage is 1.7 mA. The simulated noise figure and gain are shown in Fig. 2.

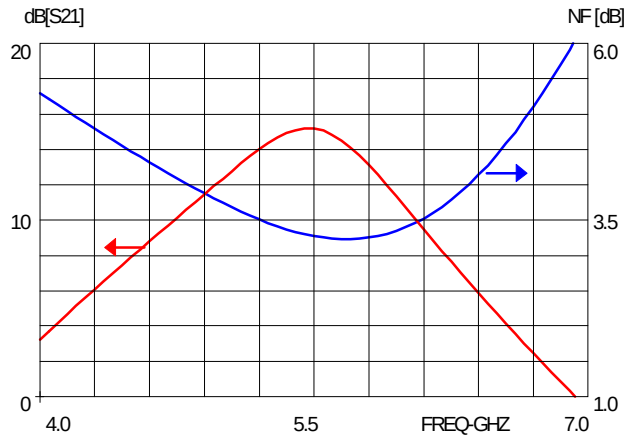

Fig. 2: Simulated noise figure and gain at 3.3 V nominal bias voltage

The chip photo is shown in Fig. 3. The chip size is 0.6 mm x 1.4 mm. The layout allows on wafer testing with signal-ground-signal probes providing RF connections as well as the single bias voltage.

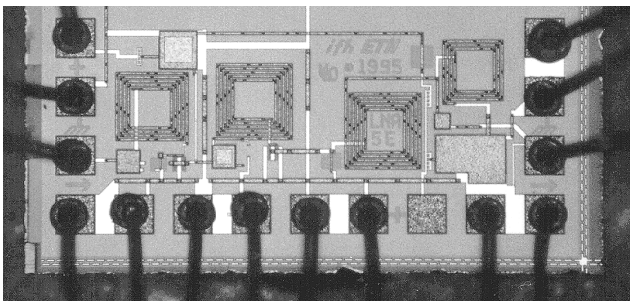

Fig.3: Microphotograph of the LNA chip (size of the active area: 0.6 mm x 1.4 mm)

MEASUREMENTS

The circuit was fabricated with the Triquint QED/A foundry process with 0.7 µm gate length. Chips from two wafers have been measured, both on wafer and in test packages. Fig. 4 shows the noise figure of a packaged chip measured with the HP8970B/HP8971C noise figure meter.

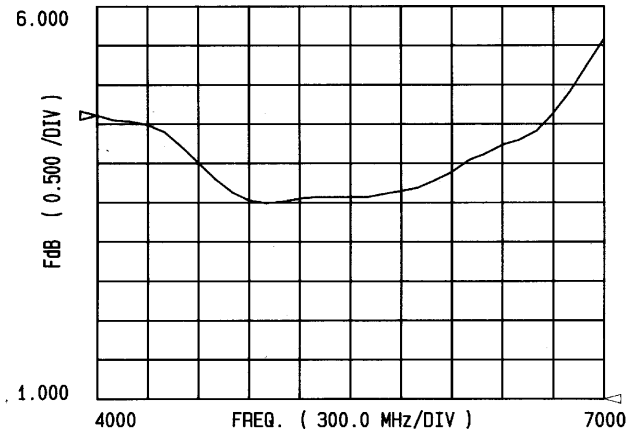

Fig. 4: Measured noise figure in a test package at a bias voltage of 3.3 V

The best noise figure of 3.5 dB is obtained at 5.0 GHz due to the longer than designed input bond wire in this test package. In the same package the gain peak is near 5.5 GHz (Fig. 5).

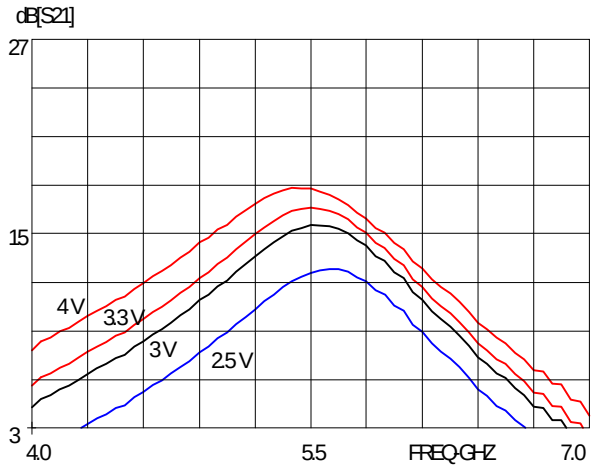

Fig. 5: Measured gain at four different supply voltages: 2.5, 3.0, 3.3 (nominal) and 4 V (measured in a test package)

The small signal gain is > 15 dB between 5.2 and 5.8 GHz at the nominal bias of 3.3 V. Fig. 5 also shows that the stability of the gain versus bias voltage variations is very good. The gain is between 12 dB at 2.5V (1.8 mA DC current) and 17 dB gain at 4 V (4 mA). The corresponding gain/P_{DC} figures of merit are 1.5 dB/mW at 3.3 V, 2.6 dB/mW at 2.5 V and 1.06 dB/mW at 4 V. With zero external input inductance, peak gain occurs close to 6 GHz.

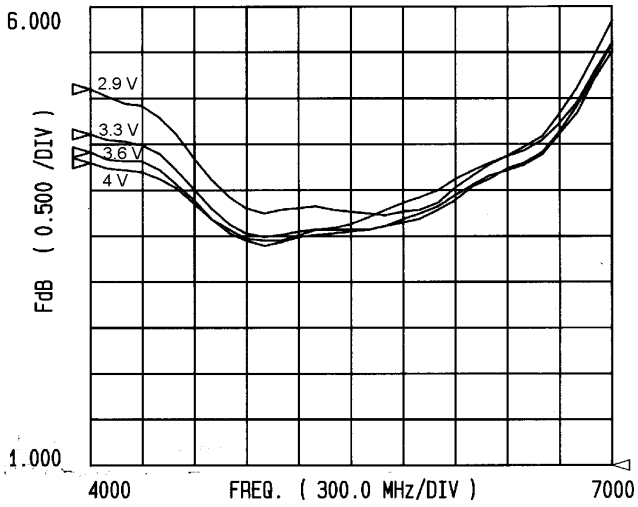

Fig. 6: Measured noise figure for different bias voltages (2.9, 3.3, 3.6 and 4 V) for the packaged low noise amplifier

The noise figure is also very insensitive to bias voltage variations as is shown in Fig. 6. Between 2.9 and 4 V, the noise figure is below 4 dB from 4.8 to 5.9 GHz for the packaged chip. According to the PCM data supplied by the foundry, the drain current I_{Do} of the E-MESFET is about 70 % of the nominal value. Due to the DC feedback the supply current is only about 10% lower than nominal, i.e. 3 mA instead of the nominal 3.4 mA. As Fig. 5 and 6 prove, the measured gain and noise figure are very close to the designed data (cf. Fig. 2).

Finally, Fig. 7 shows that the circuit is also robust against process variations. The noise figure varies less than 0.25 dB over 10 randomly selected chips from two different wafers. The ripple in this measurement is due to the uncorrected reflections of the wafer probes.

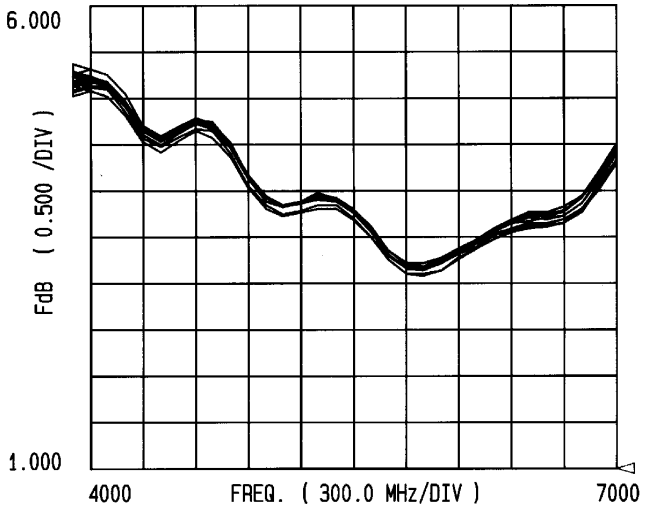

Fig. 7: Variation of the noise figure for 10 different chips from two wafers (on wafer tested)

An important feature of LNAs for short range wireless data applications is good compression and intermodulation performance. Systems like Hiperlan require from the receiver to operate at input power levels up to -20 dBm.
For amplifier circuits lower DC power consumption generally also means lower compression point. The designed amplifier has a measured -1 dB input compression point of -21 dBm (Fig. 8), which equals an output compression point of -7 dBm.

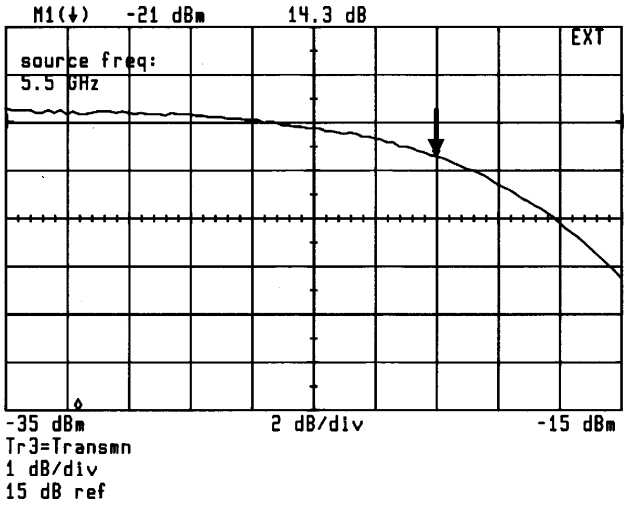

Fig. 8: Measured gain compression of the low power LNA at 5.5 GHz with 3.3 V bias (Marker M1 indicates the -1dB compression input power of -21 dBm, where the is gain 14.3 dB)

Table 1 gives a summary of the performance data of the amplifier over the Hiperlan and ISM frequency range.

Table 1: Data of the 5 GHz LNA chip at 3.3V bias

	minimum	maximum	unit
frequency range	5.0	6.0	GHz
gain	12	16.5	dB
noise figure	3.5	4.0	dB
input -1dB compression point	-21		dBm
input return loss		-5	dB
output return loss		-9	dB
reverse isolation		-25	dB
supply current	2.9	3.4	mA

CONCLUSIONS

A monolithic LNA for wireless data applications at 5.2 to 5.8 GHz was designed and measured. It has shown a noise figure of 3.5 dB and 15 dB gain at 3.3 V supply voltage, consuming only 3 mA of current. Thus, a very high gain/P_{DC} figure of merit of 1.5 dB/mW is achieved. Despite the use of enhancement devices, the circuit is very stable against supply voltage and process variations.

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